Kodak

DEVICE
PERFORMANCE
SPECIFICATION

KAF-4320E

2084 (H) x 2084 (V)
Enhanced Response Full-Frame
CCD

April 19, 2004
Revision 1.0

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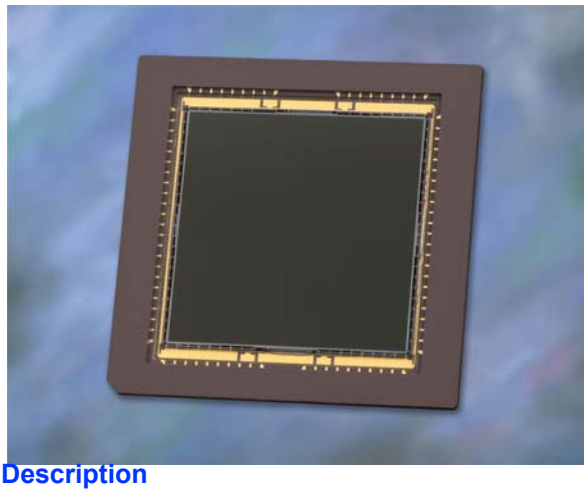
SUMMARY SPECIFICATION

KODAK KAF-4320E Image Sensor 2084 (H) x 2084 (V) Enhanced Response Full-Frame CCD



Description

The KAF4320E is a high performance monochrome area CCD (charge-coupled device) image sensor with 2084 x 2084V photoactive pixels. It is designed for a wide range of image sensing applications in the 350 nm to 1000 nm wavelength band. Typical applications include military, scientific, and industrial imaging. A dynamic range of >32,000:1 is possible with read out time less than 0.5 seconds.

The sensor is built with a true two-phase CCD technology employing a transparent gate. This technology simplifies the support circuits that drive the sensor, reduces the dark current without compromising charge capacity, and significantly increases to optical response compared to traditional front illuminated full frame sensors.

Twenty-four micron pixels are arranged into an array of 2084x2084 photosites. One quarter of the image is read from each of four outputs. Each output is driven by a low impedance two stage source follower that provides a high conversion gain, allowing low noise at pixel rates of 3MHz per output (net readout rate of 12MHz)

Revision No. 1.0
Effective Date: April 19, 2004

Parameter	Value
Architecture	Full-Frame CCD; Enhanced Response
Total Number of Pixels	2092 (H) x 2092 (V)
Number of Active Pixels	2084 (H) x 2084 (V) = approx. 4.3M
Pixel Size	24.0µm (H) x 24.,0µm (V)
Imager Size	50.02(H)mm x 50.02(V)mm
Die Size	8.4mm (H) x 5.5mm (V)
Read Noise	20 electrons (3 MHz)
Saturation Signal	500,000 electrons
Quantum Efficiency	Peak: 65%
Output Sensitivity	10 µV/e
Outputs	4
Dark Current	<15pA/cm^2 @ 25°C
Dark Current Doubling Temperature	6.4°C
Dynamic Range	> 20,000 : 1
Blooming Suppression	None
Maximum Data Rate	3 MHz

DEVICE DESCRIPTION

Architecture

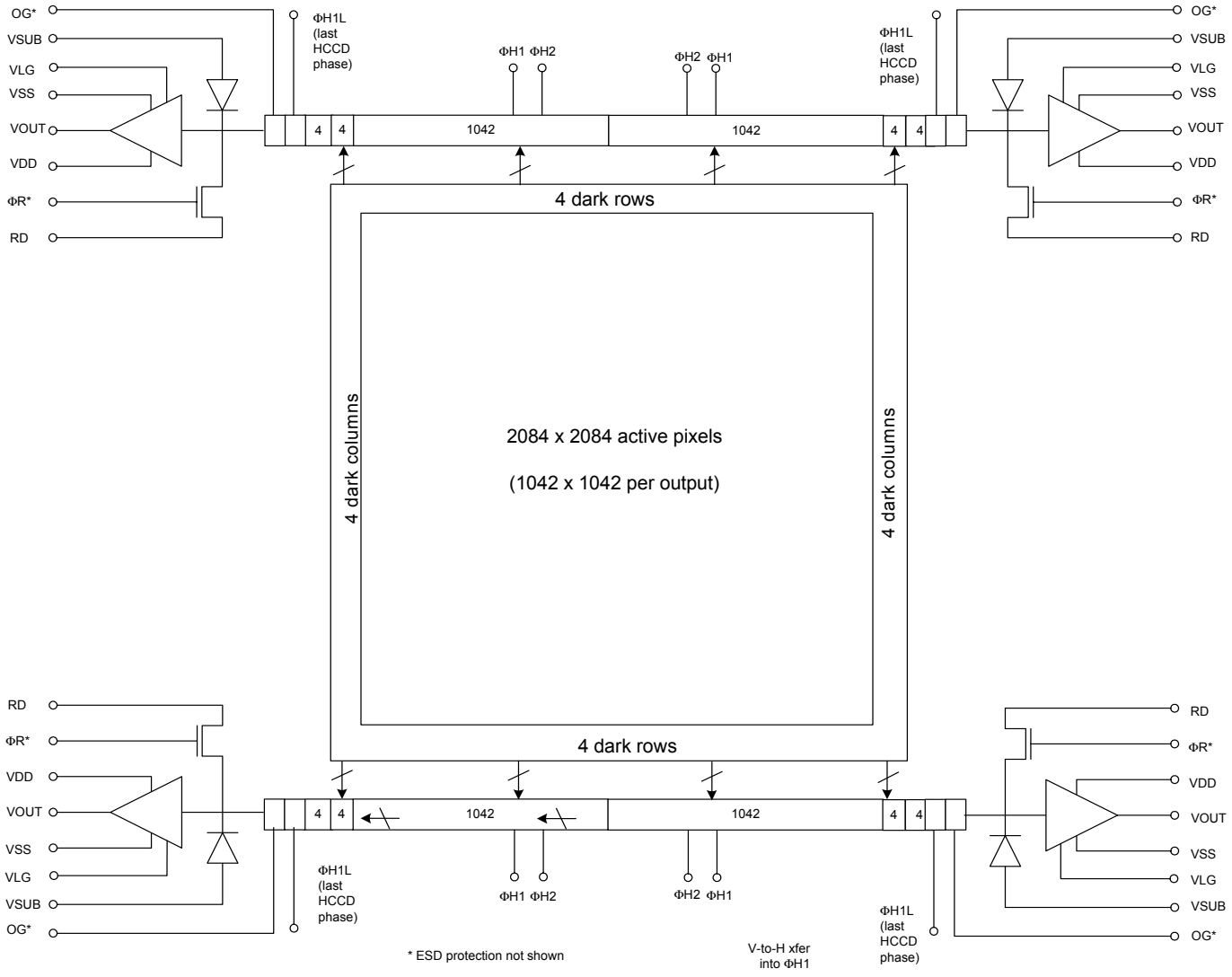


Figure 1 Functional block diagram

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the ΦV1 and ΦV2 register clocks are held at a constant (low) level. See Figure 14 Timing diagrams.

Charge Transport

Referring again to “Figure 14 Timing diagrams”, the integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD to the horizontal CCD register using the ΦV1 and ΦV2 register clocks. The horizontal CCD is presented a new line on the falling edge of ΦV2 while ΦH1 is held high. The horizontal CCD then transports each line, pixel by pixel, to the output structure by alternately clocking the ΦH1 and ΦH2 pins in a complementary fashion. On each falling edge of ΦH1L a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

Output Structure

Charge presented to the floating diffusion is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the floating diffusion. Once the signal has been sampled by the system electronics, the reset gate (ΦR) is clocked to remove the signal and the floating diffusion is reset to the potential applied by Vrd. (see figure Figure 2 Output schematic). More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device such as shown in Fig 4.

If charge binning is desired, the charge can be combined at the output node or it can be combined in the ΦH1L gate and then presented to the output node.

Dark Reference Pixels

There are 4 light shielded pixels at the beginning of each line. There are 4 dark lines at the start of every frame and 4 dark lines at the end of each frame. Since there are outputs at each of the four, corners, the light shield will affect the beginning of each line from each output, and for the first four lines from each of the outputs. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

Dummy Pixels

Within the horizontal shift register are 4-1/2 leading pixels that are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions.

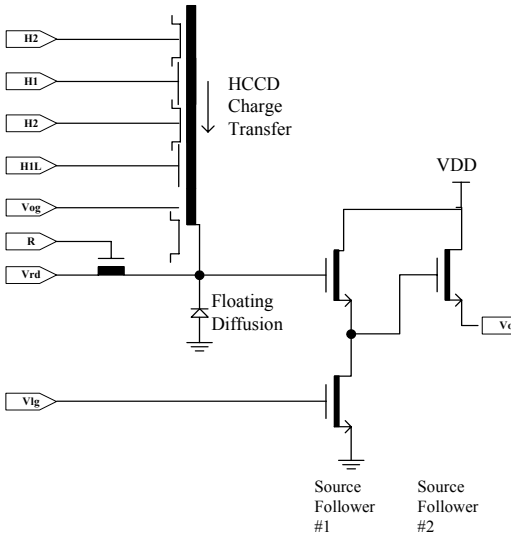


Figure 2 Output schematic

Physical Description

Pin Description

Table 1 - Pin descriptions

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Substrate (ground)	43	VRD	Reset Drain
2	ϕR	Reset Clock	44	GND	Substrate (ground)
3	VOG	Output gate bias	45	ϕR	Reset Clock
4	ϕH1L	Horizontal CCD Clock – Last phase	46	VOG	Output gate bias
5	ϕH1	Horizontal CCD Clock – Phase 1	47	ϕH1L	Horizontal CCD Clock – Last phase
6	ϕH2	Horizontal CCD Clock – Phase 2	48	ϕH1	Horizontal CCD Clock – Phase 1
7	GND	Substrate (ground)	49	ϕH2	Horizontal CCD Clock – Phase 2
8	GND	Substrate (ground)	50	GND	Substrate (ground)
9	GND	Substrate (ground)	51	GND	Substrate (ground)
10	N/C	No connect	52	GND	Substrate (ground)
11	N/C	No connect	53	GND	Substrate (ground)
12	GND	Substrate (ground)	54	GND	Substrate (ground)
13	GND	Substrate (ground)	55	GND	Substrate (ground)
14	GND	Substrate (ground)	56	ϕH2	Horizontal CCD Clock – Phase 2
15	ϕH2	Horizontal CCD Clock – Phase 2	57	ϕH1	Horizontal CCD Clock – Phase 1
16	ϕH1	Horizontal CCD Clock – Phase 1	58	ϕH1L	Horizontal CCD Clock – Last phase
17	ϕH1L	Horizontal CCD Clock – Last phase	59	VOG	Output gate bias
18	VOG	Output gate bias	60	ϕR	Reset Clock
19	ϕR	Reset Clock	61	GND	Substrate (ground)
20	GND	Substrate (ground)	62	VRD	Reset Drain
21	VRD	Reset Drain	63	VSS	Amplifier Supply Return
22	VSS	Amplifier Supply Return	64	VLG	Source follower load gate bias
23	VLG	Source follower load gate bias	65	GND	Substrate (ground)
24	GND	Substrate (ground)	66	Vout4	Amplifier output
25	Vout2	Amplifier output	67	VDD	Amplifier Supply
26	VDD	Amplifier Supply	68	ϕ_{V2}	Vertical CCD Clock -Phase 2
27	ϕ_{V2}	Vertical CCD Clock - Phase 2	69	ϕ_{V1}	Vertical CCD Clock - Phase 1
28	ϕ_{V1}	Vertical CCD Clock - Phase 1	70	GND	Substrate (ground)
29	GND	Substrate (ground)	71	ϕ_{V1}	Vertical CCD Clock - Phase 1
30	ϕ_{V1}	Vertical CCD Clock -	72	ϕ_{V2}	Vertical CCD Clock - Phase 2

Pin	Symbol	Description	Pin	Symbol	Description
		Phase 1			
31	ϕ_{V2}	Vertical CCD Clock - Phase	73	Guard	Guard Ring
32	Guard	Guard Ring	74	ϕ_{V2}	Vertical CCD Clock - Phase
33	ϕ_{V2}	Vertical CCD Clock - Phase	75	ϕ_{V1}	Vertical CCD Clock - Phase 1
34	ϕ_{V1}	Vertical CCD Clock - Phase 1	76	GND	Substrate (ground)
35	GND	Substrate (ground)	77	ϕ_{V1}	Vertical CCD Clock - Phase 1
36	ϕ_{V1}	Vertical CCD Clock - Phase 1	78	ϕ_{V2}	Vertical CCD Clock - Phase 2
37	ϕ_{V2}	Vertical CCD Clock - Phase	79	VDD	Amplifier Supply
38	VDD	Amplifier Supply	80	Vout1	Amplifier output
39	Vout3	Amplifier output	81	GND	Substrate (ground)
40	GND	Substrate (ground)	82	VLG	Source follower load gate bias
41	VLG	Source follower load gate bias	83	VSS	Source follower load gate bias
42	VSS	Amplifier Supply Return	84	VRD	Reset Drain

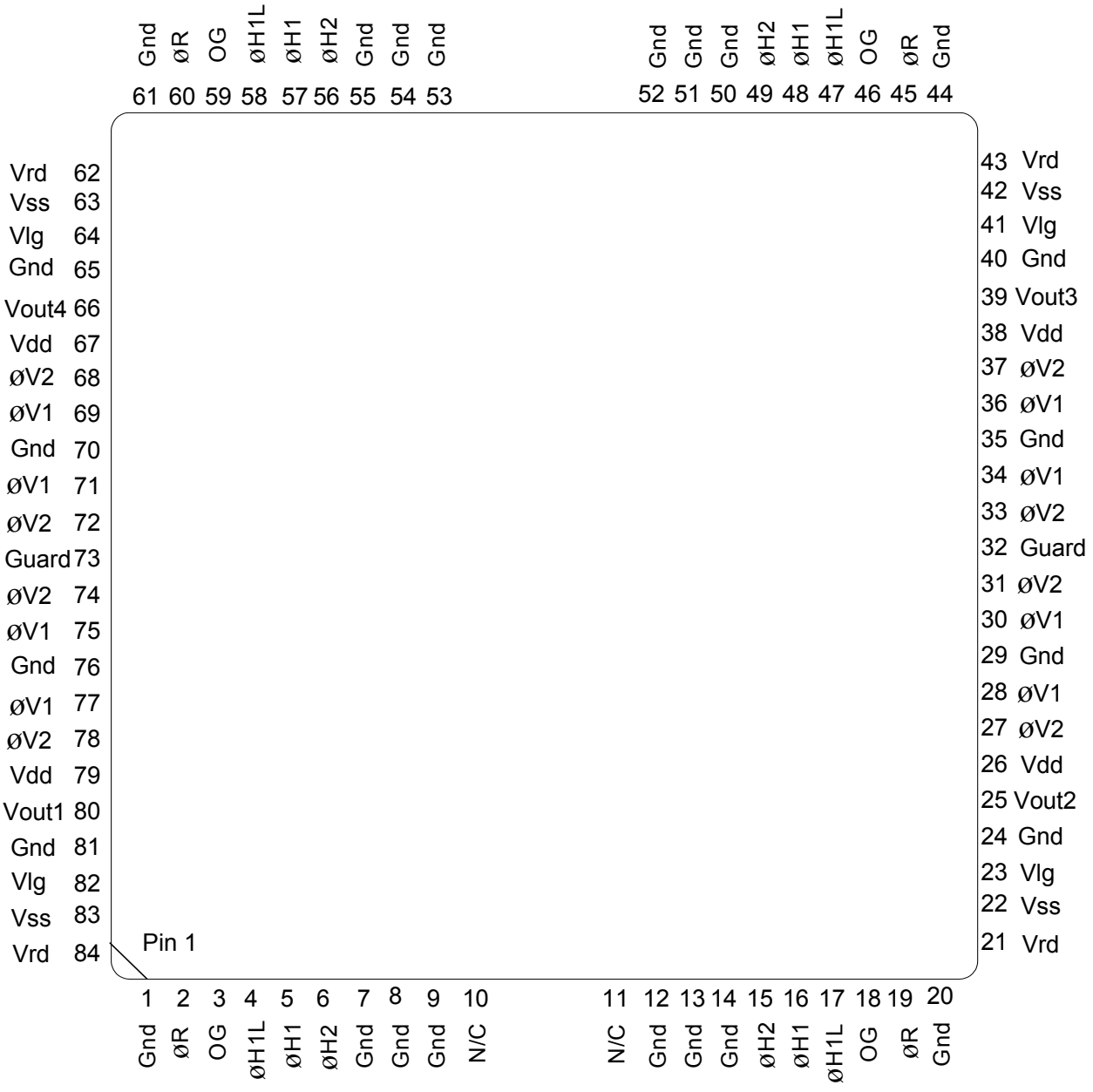


Figure 3 Package pin designation

Performance

Electro Optical Specifications

All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Saturation Signal **Vertical CCD capacity** **Horizontal CCD capacity** **Output Node capacity**	Nsat	500000	650000 850000 550000		electrons / pixel	1
Quantum Efficiency (see Figure 4 Spectral response)						
Photoresponse Non-Linearity	PRNL		< 1.0	2.0	%	2
Photoresponse Non-Uniformity	PRNU		0.8	2.0	%	3
Channel to channel Gain Difference	ΔG		0.2	5	%	10
Dark Signal	Jdark		250 7	540 15	electrons / pixel / sec pA/cm^2	4
Dark Signal Doubling Temperature			6.3	7	°C	
Dark Signal Non-Uniformity	DSNU		300	540	electrons / pixel / sec	5
Dynamic Range	DR	86	87.5		dB	6
Charge Transfer Efficiency	CTE	0.99997	0.99999			8
Output Amplifier DC Offset	Vodc	Vrd	Vrd + 1	Vrd + 2	V	
Output Amplifier Sensitivity	Vout/Ne~	9	10	11	uV/e~	
Output Amplifier output Impedance	Zout		150		Ohms	
Noise Floor	ne~		17	24	electrons	7

Notes:

1. The maximum output video amplitude limits the charge capacity and dynamic range. The maximum charge capacity is determined from a photon transfer measurement and is defined as the point where the mean-variance fails to demonstrate the theoretical behavior.
2. Worst case deviation from straight line fit, between 0.1% and 95% of Vsat.
3. One Sigma deviation of a 1042 x 1042 sample (data from one output) when the CCD is illuminated uniformly at half of saturation, excluding defective pixels. [100 * (std deviation/average)]
4. Average of all pixels with no illumination at 25°C.
5. Average dark signal of any of 16 x 16 blocks within the sensor (each block is 130x 130 pixels).
6. The dynamic range limited by the noise of the output amplifier (i.e. at temperatures less than –10 C) , pixel frequency = 3MHz, bandwidth = 10 MHz.
7. Noise floor of the CCD amplifier assuming correlated double sampling, pixel frequency = 3MHz, and bandwidth = 10MHz.
8. Signals > 1% of well Vsat.
9. ΔG = abs(100 * (1 – [response of a channel]/ [average response of all four channels])). The specified gain difference is the combination of all the gain errors on the CCD sensor and the analog signal processing in the test system.

Spectral Response

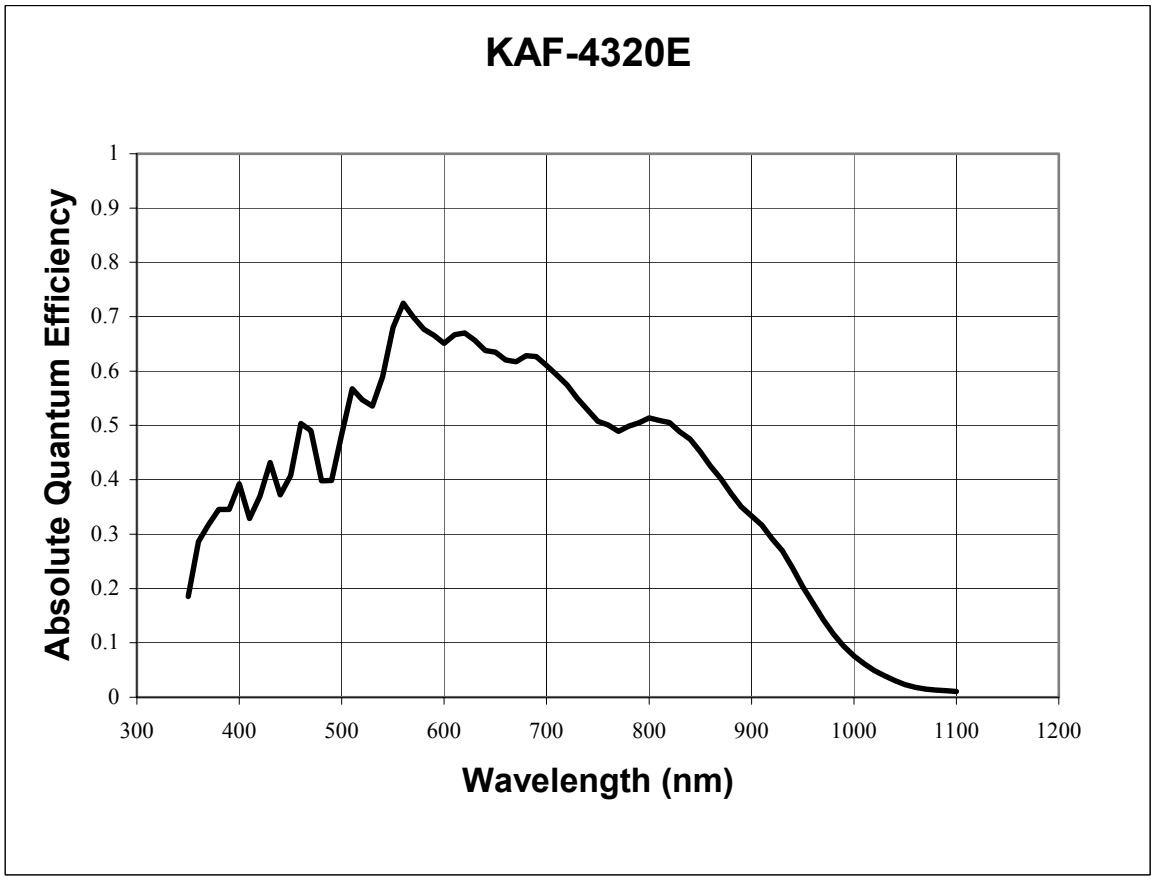


Figure 4 Spectral response

Dark Current

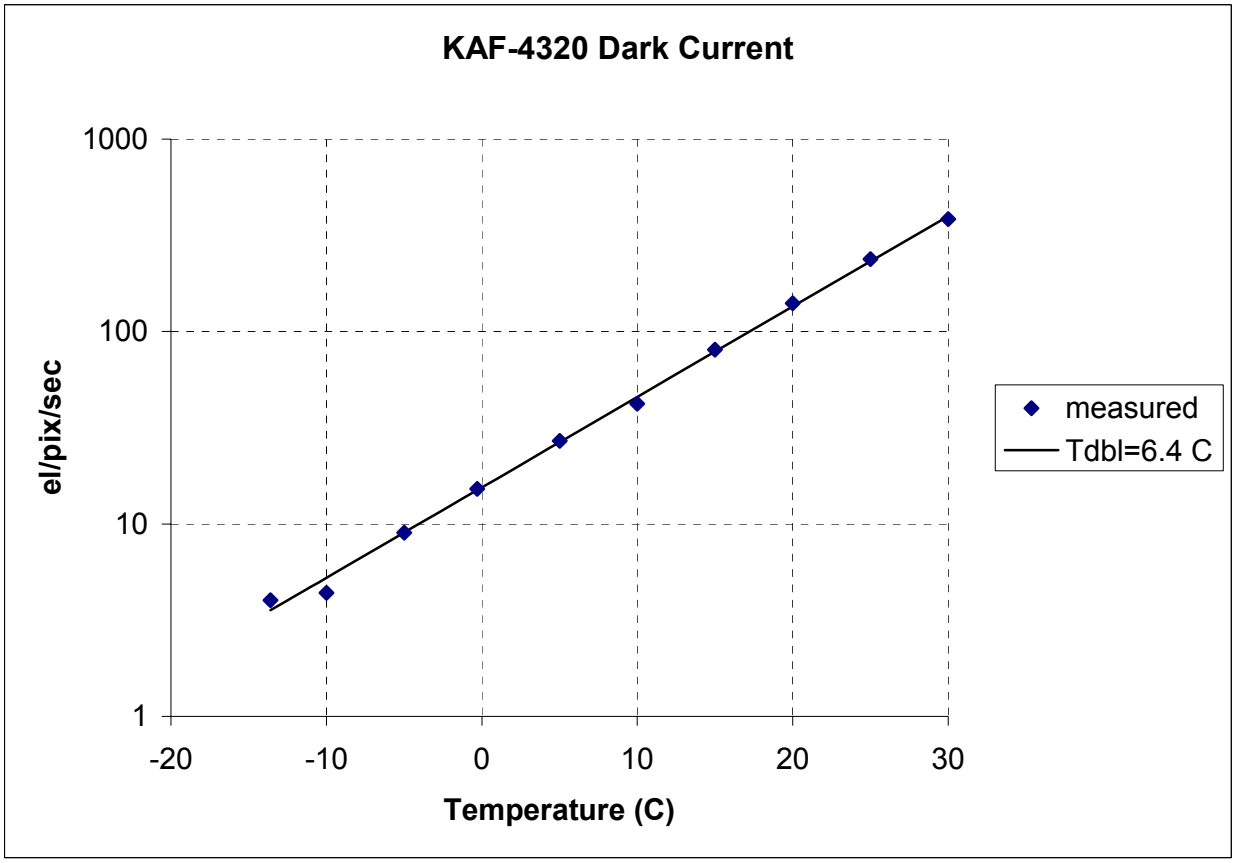


Figure 5 Dark current temperature dependence

Linearity

Figure 6 Linearity shows a typical result from measuring the signal response as a function of integration time, while the illumination level is constant. The data is fit in log space to give equal weighting between low and high signal levels. A perfectly linear system would have a slope of 1.00 in log space. The slope in the fit is allowed to deviate from the ideal by a small amount. Typical values of the slope are between 1.00 and 1.02. The deviation from linear is defined as :

%dev = abs(100 * [measured value-fit value]/ fit value).

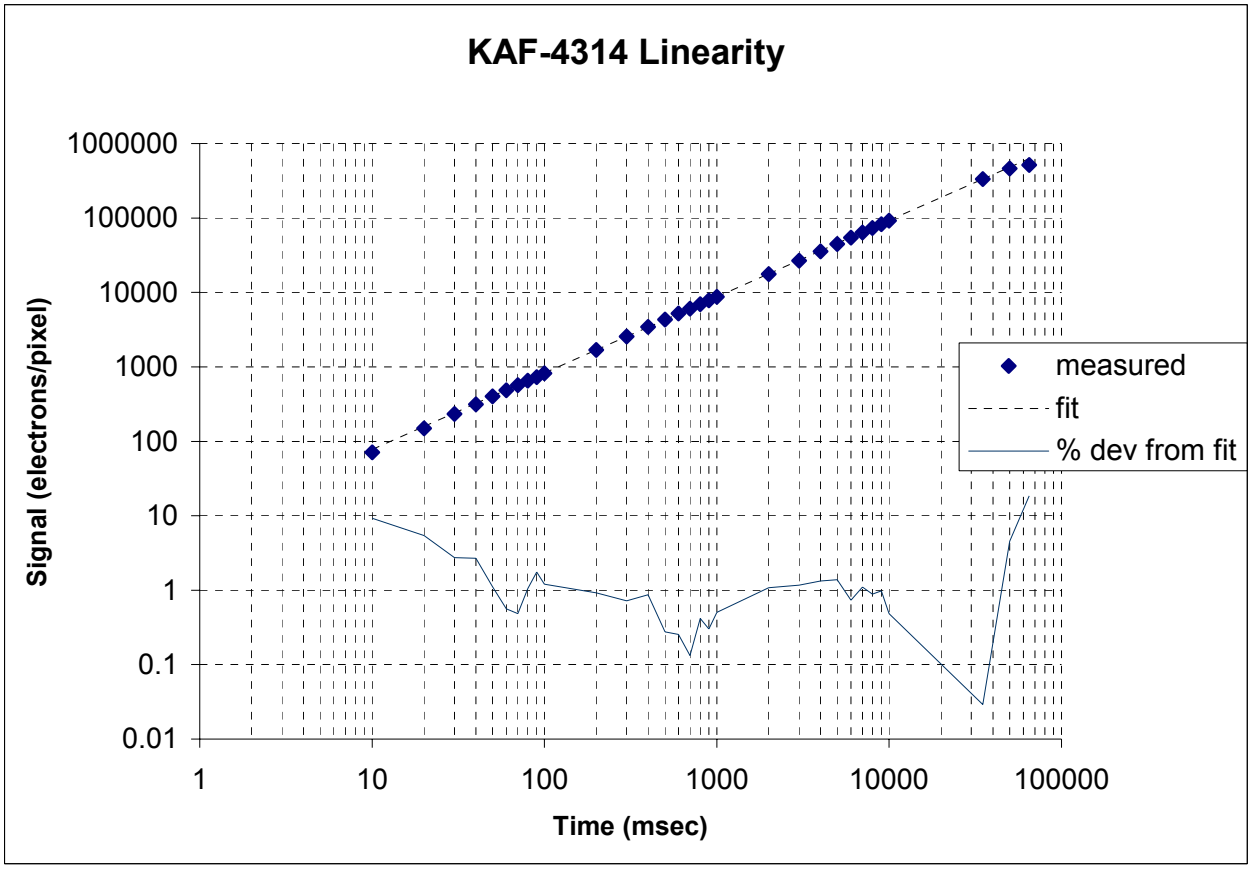


Figure 6 Linearity

CCD Output

The following figures show typical CCD video at the output of the CCD and at the input of the analog to digital converter (A/D) in the test system. Bandwidth limiting is applied at the A/D input to minimize the noise floor.

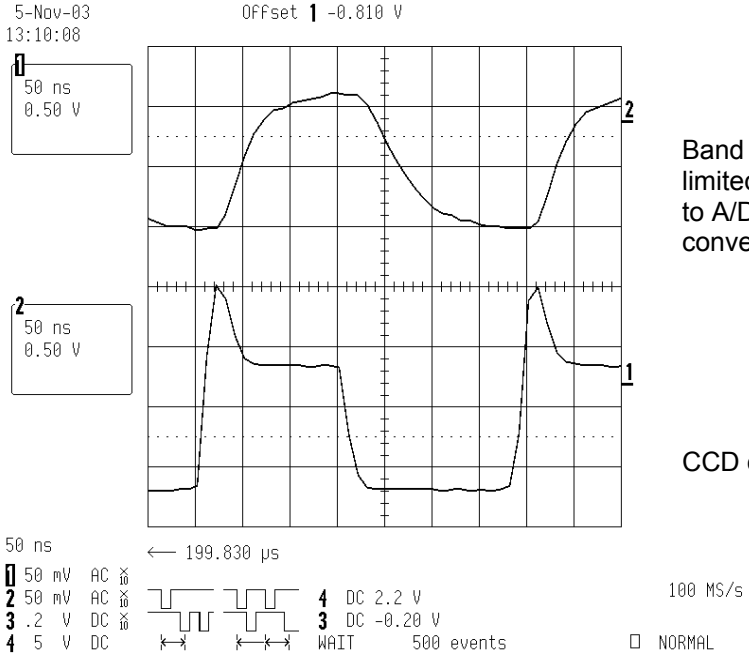


Figure 7 CCD output : small signal

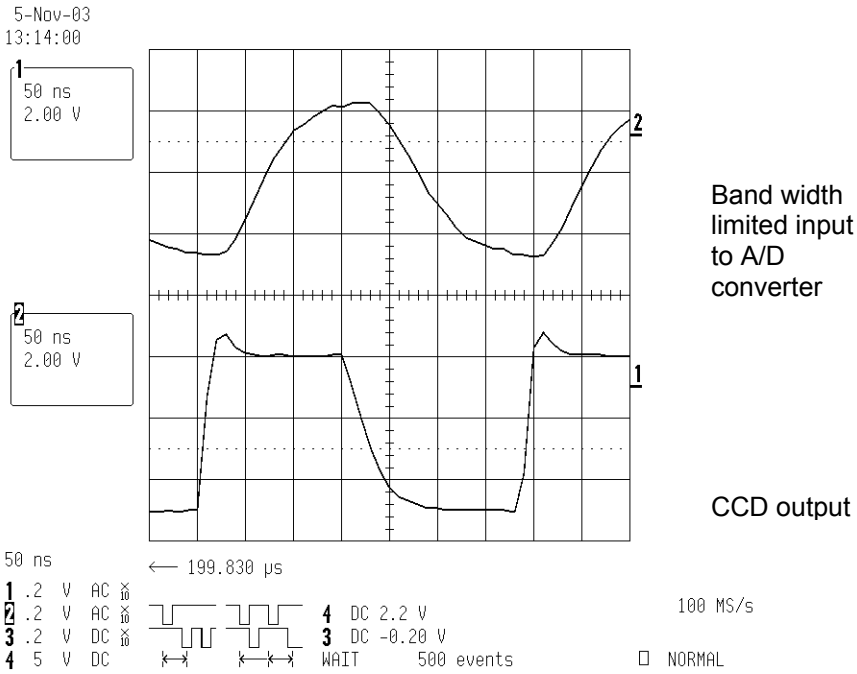


Figure 8 CCD output Large signal

Noise

The CCD amplifier noise floor, the CCD dark current during readout, and other system components such as the analog-digital converter dictate the total system noise.

CCD amplifier

The noise contributed by the output amplifier is determined from the amplifier's noise power spectrum, the system bandwidth, and any other analog processing. Correlated double sampling is a standard analog processing technique used with CCDs and it is assumed that it is used for all of the rest of the calculations and results in this document.

System noise

The total noise will be the combination of the CCD and the noise contributed by other components in the processing circuitry. The total noise, dominated by the CCD and the A/D converter is also shown in Figure 9 Noise versus pixel rate". The measured vales were obtained using a system that employed Datel 16 bit analog to digital converters, the ADS 931 and ADS933. The system noise obtained matched the Datel specifications exactly and was similar and slightly lower than the CCD noise contribution. The table below shows the results and good agreement between the expected and measured results for the CCD alone and the CCD in the system at 1MHz and 3 MHz. The values in the table are in electrons referred to the CCD amplifier input.

Frequency	CCD Measured Noise	CCD+System Datel ADS93x measured
1.00E+06	12	16.2
3.00E+06	17.3	22.6

Temperature dependence of the noise floor

The temperature dependence of the noise floor is dictated primarily by the dark current generated during the readout time for the CCD. Figure 10 Noise versus temperature - 3 MHz pixel rate" and Figure 11 Noise versus temperature - 1 MHz pixel rate" show the expected dynamic range of the KAF-4320E as a function of temperature for two pixel rates, 1MHz and 3 MHz. The dynamic range was calculated using the measured amplifier and system noise values, the expected dark current performance, and the saturation signal of the KAF-4320E. At 25 C the dark current shot noise can contribute from 12 to 50 electrons and dominate the noise floor. The maximum dynamic range can be achieved at temperatures < -10 C for these read out frequencies.

Noise versus Frequency

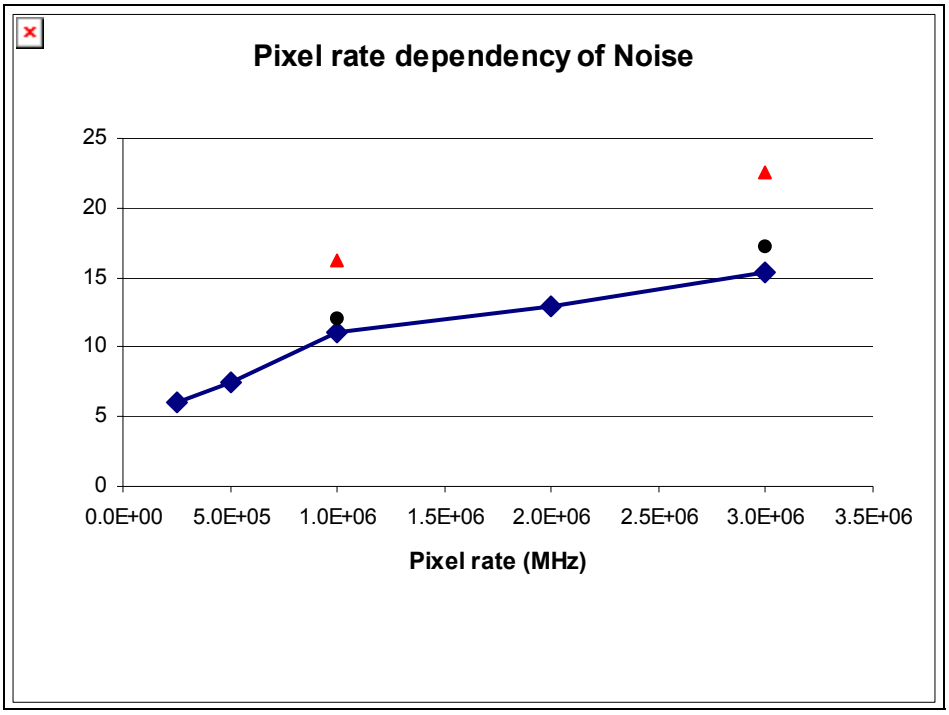


Figure 9 Noise versus pixel rate

Performance versus temperature

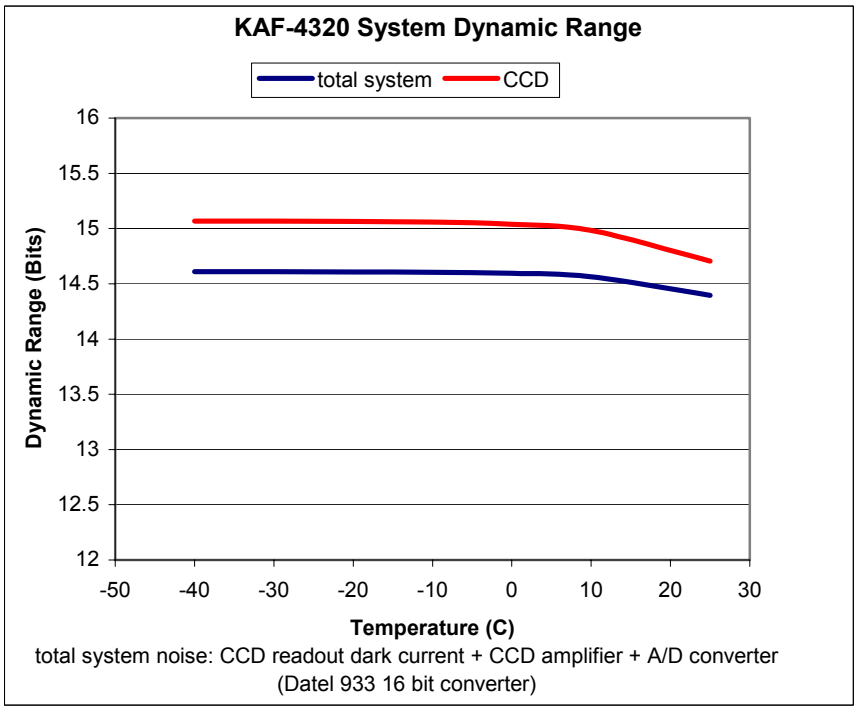


Figure 10 Noise versus temperature - 3 MHz pixel rate

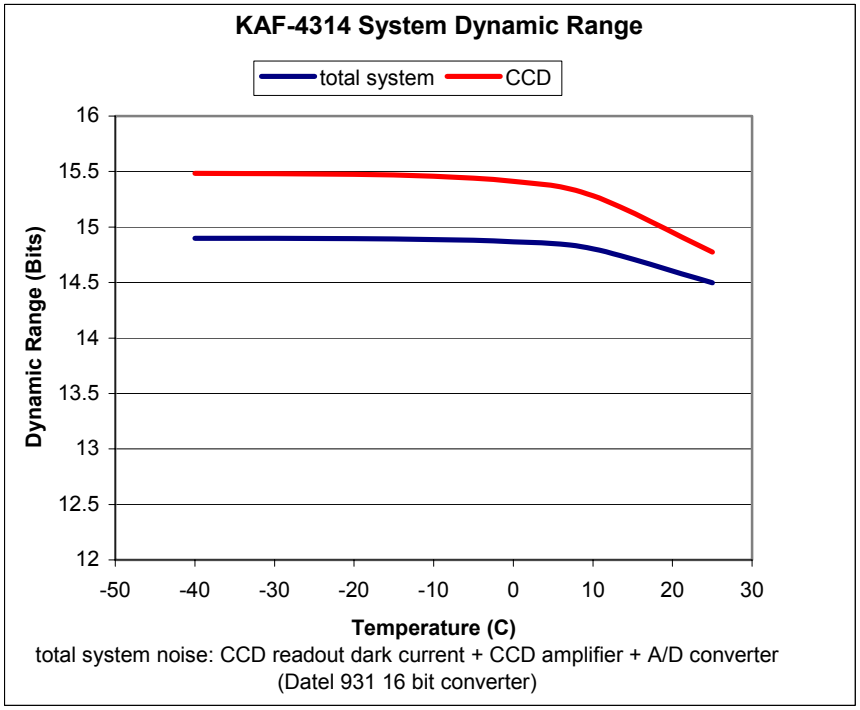


Figure 11 Noise versus temperature - 1 MHz pixel rate

Cosmetic Specification

Cosmetic tests performed at T=25°C

Grade	Point Defects	Cluster Defects	Columns	Double Column
C1	≤50	≤20	0	0
C2	≤100	≤20	≤4	0

Cosmetic Definitions

Point Defect	DARK: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation, OR BRIGHT: A Pixel with dark current > 5000 e/pixel/sec at 25C.
Cluster Defect	A grouping of not more than 5 adjacent point defects.
Column Defect	1) A grouping of >5 contiguous point defects along a single column. 2) A column containing a pixel with dark current > 150,000e/pixel/sec (bright column). 3) A column that does not meet the minimum vertical CCD charge capacity (low charge capacity column). 4) A column which loses more than 500 e under 2Ke illumination (trap defect).
Neighboring pixels	The surrounding 128 x 128 pixels or ±64 columns/rows.
Defect Separation	Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).

Cluster defects are separated by no less than 2 pixels from other column and cluster defects.
Column defects are separated by no less than 5 pixels from other column defects.

Operation

Absolute Maximum Ratings

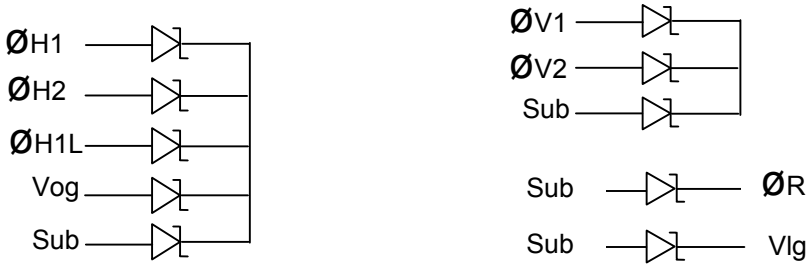
Description	Symbol	Min.	Max.	Units	Notes
Diode Pin Voltages	Vdiode	0	25	V	1,2
Gate Pin Voltages –Type 1	Vgate1	-17	17	V	1,3,7
Gate Pin Voltages – Type 2	Vgate2	0	17	V	1,4,7
Output Bias Current	Iout		-10	mA	5
Output Load Capacitance	Cload		15	pF	5
Storage Temperature	T		100	°C	
Humidity	RH	5	90	%	6

Notes:
1. Referenced to pin Vsub or between each pin in this group.
2. Includes pins: Vrd, Vdd, Vss, Vout.
3. Includes pins: ϕV1, ϕV2, ϕH1, ϕH2, ϕH1L,
4. Includes pins: Vog, Vlg. ϕR.
5. Avoid shorting output pins to ground or any low impedance source during operation.
6. T=25°C. Excessive humidity will degrade MTTF.
7. This sensor contains gate protection circuits to provide protection against ESD events. The circuits will turn on when greater than 18 volts appears between any two gate pins. Permanent damage can result if excessive current is allowed to flow under these conditions.

CAUTION:	**This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance with strict ESD procedures for Class 0 devices (JESD22 Human Body Model) or Class A (Machine Model). Refer to Application Note MTD/PS-0224, "Electrostatic Discharge Control"**

Equivalent Input Circuits

Many of the pins contain a form of gate protection to prevent damage from electrostatic discharge. These take the form of zener diodes that prevent the voltage differences between gates from becoming large enough to damage the sensor. Isolated gates such as ØR, and Vlg require only protection between the gate and the sensor substrate.



DC Operating Conditions

Description	Symbol	Min.	Nom.	Max	Units	Max DC Current (mA)	Notes
Reset Drain	Vrd		18.5		V	0.01	2
Output Amplifier Return	Vss		2.0		V	1	3
Output Amplifier Supply	Vdd		21		V	Iout	2
Substrate	GND		0		V		
Output Gate	Vog		0		V	0.01	3
Output amplifier load gate	Vlg		Vss+1.0		V	0.01	2
Guard ring	Vguard		10		V		3
Amplifier Output Current	Iout		-5	-10	mA	-	1

Notes:
1. An output load sink must be applied to Vout to activate output amplifier - see Figure below.
2. Voltage tolerance is 2% (actual voltage should be nominal +/- tolerance)
3. Voltage tolerance is 5% (actual voltage should be nominal +/- tolerance)

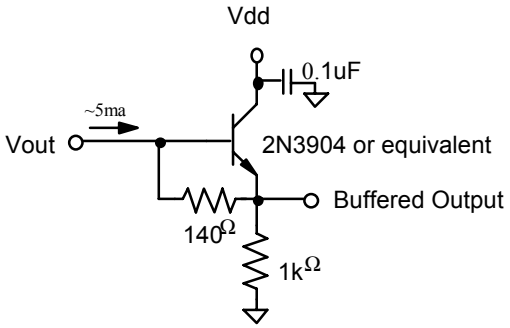


Figure 12 Example Output Structure Load Diagram. This provides a constant current source for the CCD 2-stage source follower circuit.

AC Operating Condition

Description	Symbol	Level	Nom.	Units	Effective Capacitance	Notes
Vertical CCD Clock - Phase 1	ϕV1	Low level Clock Amplitude	-8.0 8.0	V V	75 nF (each of ØV1 pins 30,34,71,75)	4,5
Vertical CCD Clock - Phase 2	ϕV2	Low level Clock Amplitude	-8.0 8	V V	75 nF (each of ØV2 pins 31,33,72,74)	4,5
Horizontal CCD Clock - Phase 1	ϕH1	Low level Clock Amplitude	0 10.0	V V	150pF (each of ØH1 pins 5,16,48,57)	3,6
Horizontal CCD Clock –Last Gate	ϕH1L	Low level Clock Amplitude	-3.0 10.0	V V	10pF	3
Horizontal CCD Clock - Phase 2	ϕH2	Low level Clock Amplitude	-3.0 10.0	V V	100pF (each of ØH2 pins 6,15,49,56)	3,7
Reset Clock	ϕR	Low level Clock amplitude	2.0 12.0	V V	5pF	3

Notes:
1. All pins draw less than 10uA DC current.
2. Capacitance values relative to VSUB.
3. Voltage tolerance is 2% (actual voltage should be nominal +/- tolerance)
4. Voltage tolerance is 5% (actual voltage should be nominal +/- tolerance)
5. Total clock capacitance is 4 * 75 nF = 300 nF.
6. Total clock capacitance is 4 * 150 pF = 600 pF
7. Total clock capacitance is 4 * 100 pF = 400 pF

AC Timing Conditions

Description	Symbol	Min.	Nom.	Max.	Units	Notes
ϕH1, ϕH2 Clock Frequency	f_H		3	3	MHz	1, 2, 3
Pixel Period (1 Count)	t_e	333	333		ns	
ϕH1, ϕH2 Setup Time	$t_{\phi HS}$	10	10		us	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	30	30		us	2
Reset Clock Pulse Width	$t_{\phi R}$		20		ns	4
Readout Time	$t_{readout}$	470.3	470.3		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	449.6	449.6		us	7

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Crossover of register clocks should be between 40-60% of amplitude.
4. ϕR should be clocked continuously.
5. $t_{readout} = (1046 * t_{line})$
6. Integration time is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7. $tline = (3 * t_{\phi V}) + t_{\phi HS} + (1050 * t_e)$

Pixel rate clock waveforms

For best performance, the horizontal clocks should be damped, similar to those shown in figure 13. The clocks in this figure were generated using a 50 ohm output impedance clock driver. Excessively fast clocks can result in a higher noise floor.

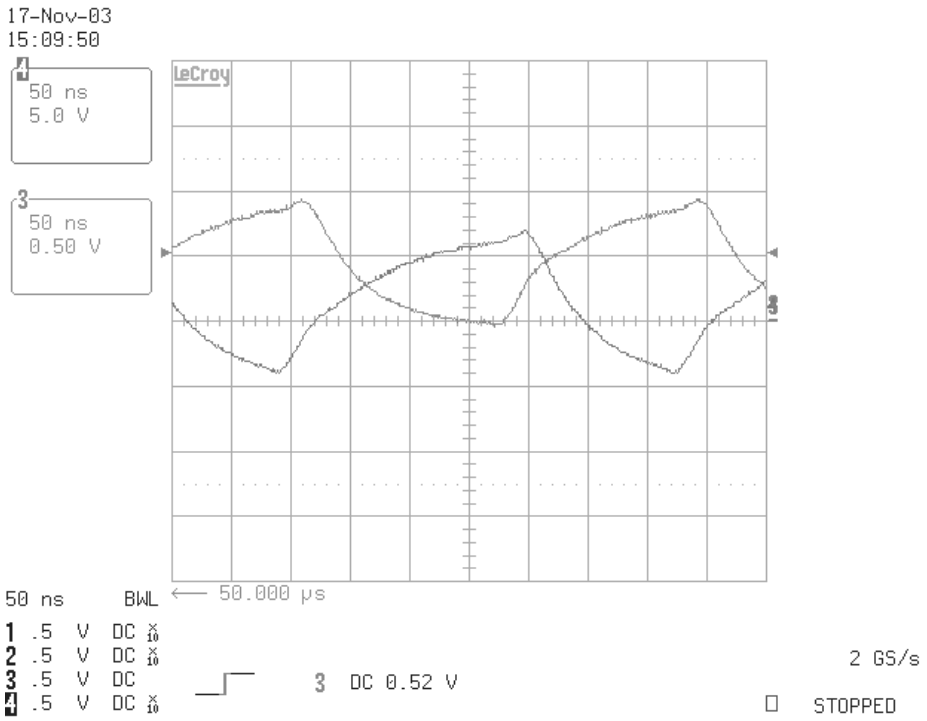
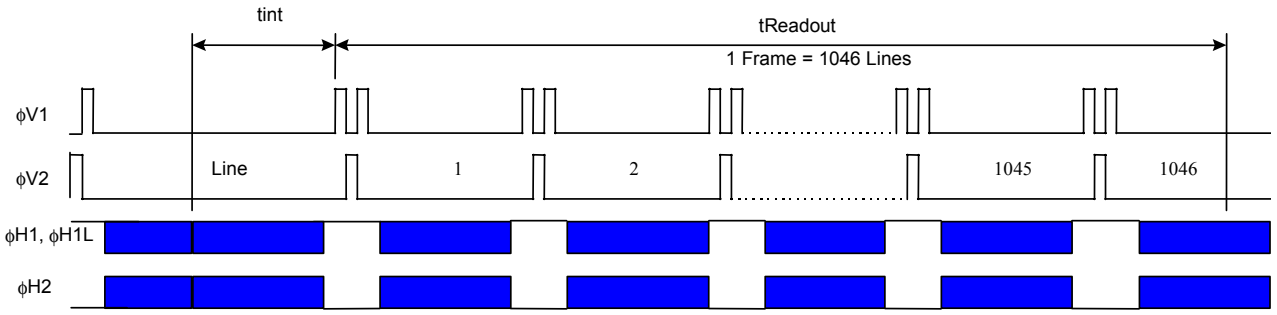


Figure 13 Clock example

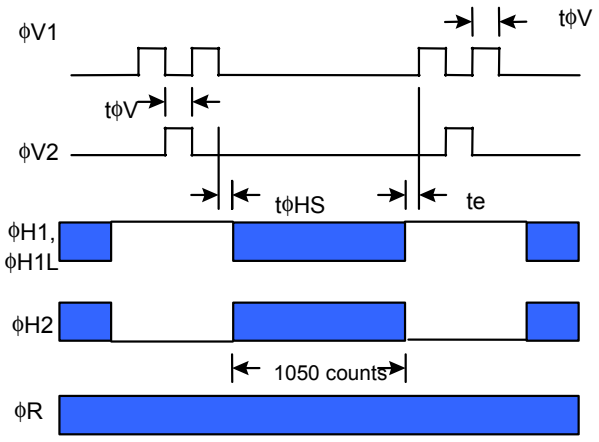
Timing Diagrams

Normal Read out

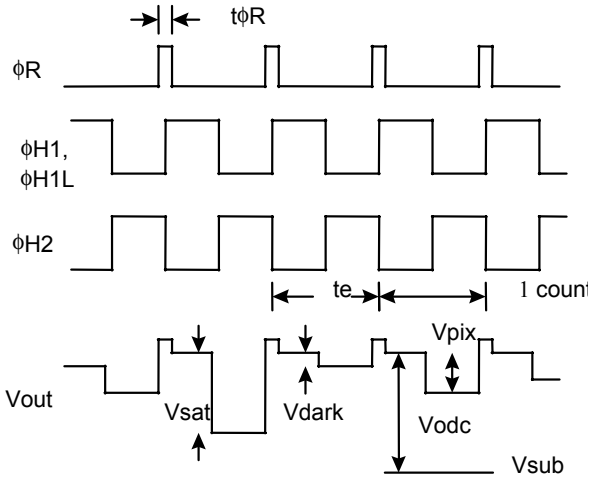
Frame Timing – per quadrant (each output contains one half of the lines)



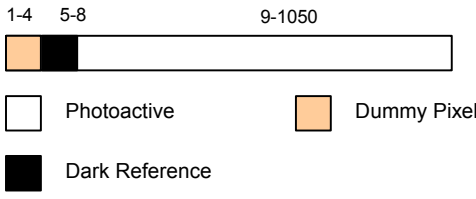
Line Timing



Pixel Timing



Line Content – per quadrant (each output contains one half of a line)



Vsat Saturated pixel video output
Vdark Video output signal in no light situation, not zero due to
Vpix Pixel video output signal level, more electrons =more
Vodc Video level offset with respect to
Vsub Analog

* See Image Aquisition section

Figure 14 Timing diagrams

Binning 2x2 Read out

Binning modes combine the signal from adjacent pixels effectively creating pixels that are sized an integral multiple of the single pixel size. The figure below shows an example for combining two lines together, then two columns together, combining the signal from four individual 24 micron pixels. For each additional line combined, one more ϕV1 and ϕV2 clock are required fro each line.

When combining columns at the output, the amplifier node is reset periodically instead of resetting at the pixel rate. The signal from successive pixels is combined at the output node for each falling edge of the H1L clock. To combine two pixels, the amplifier is reset and the output node clamped in the correlated double sampling circuit (CDS). Then H1L cycles twice, and the signal is sampled in the CDS circuit.

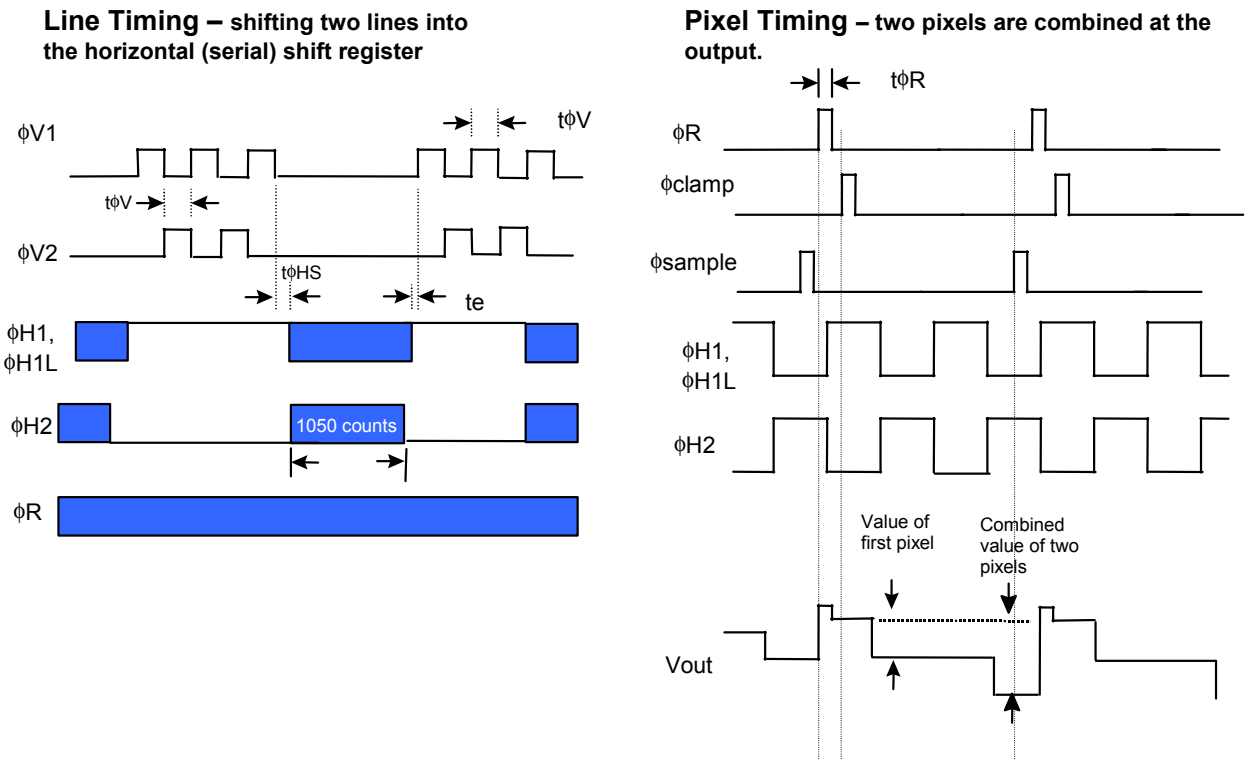


Figure 15 Timing diagram for 2x2 binning

Power Dissipation

Clock power

The power dissipated by the CCD clocks is calculated using the formula:

Power = CV^2f

Where C is the capacitance in farads, V is the clock amplitude in volts, and f is the frequency in Hz.

Amplifier power

The power dissipated by amplifiers is calculated by Power = I*V where I is the current and V is the voltage drop on the CCD. The sensor contains two stage source followers. The first stage draws approximately 250 micro amps and the voltage drop is Vdd – Vss. The second stage sources much more current, approximately 5mA while the voltage drop on the sensor is much smaller, Vdd – Vout where Vout ~ Vrd.

Total Power

The table below shows the power dissipated at three different pixel frequencies. For each of these cases the amplifier operating conditions are held constant so its contribution is not frequency dependent. The time for the vertical clock transfers is also held constant (90 microseconds per line) but the line time changes depending on the pixel rate.

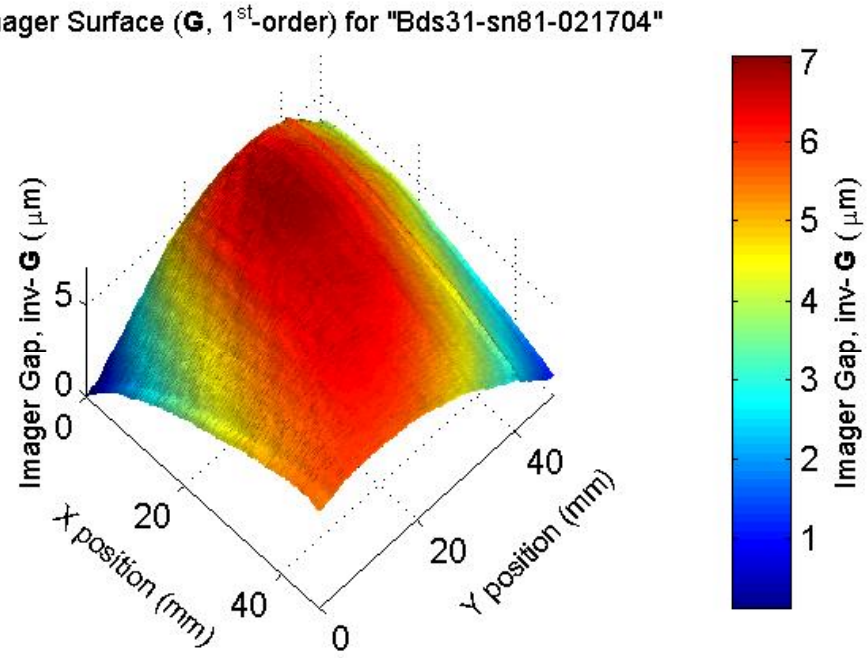
Contributor	**Pixel rate**			**Notes**
	500 kHz	1 MHz	3MHz	Pixel rate
Amplifiers	120 mW	120 mW	120 mW	Total of 4 outputs
Hccd	60 mW	120 mW	360 mW	
Vccd	62 mW	121 mW	297 mW	
Total	*241 mW*	*361 mW*	*776 mW*	

CCD Surface Flatness

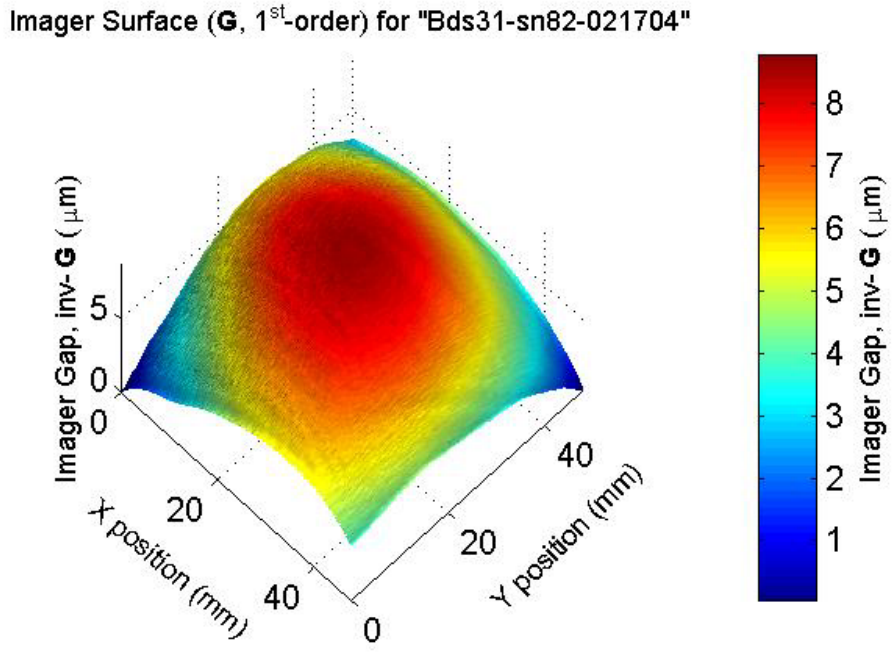
The flatness of the die is defined as a peak-to-peak distortion in the image sensor surface. The parallelism between the image sensor surface and any of the package components is not specified or guaranteed. The non-parallelism is removed when measuring the distortion in the image sensor surface.

		Min.	Nom.	Max.	Units
Die Flatness	Peak to peak distortion		8.8	12.0	microns

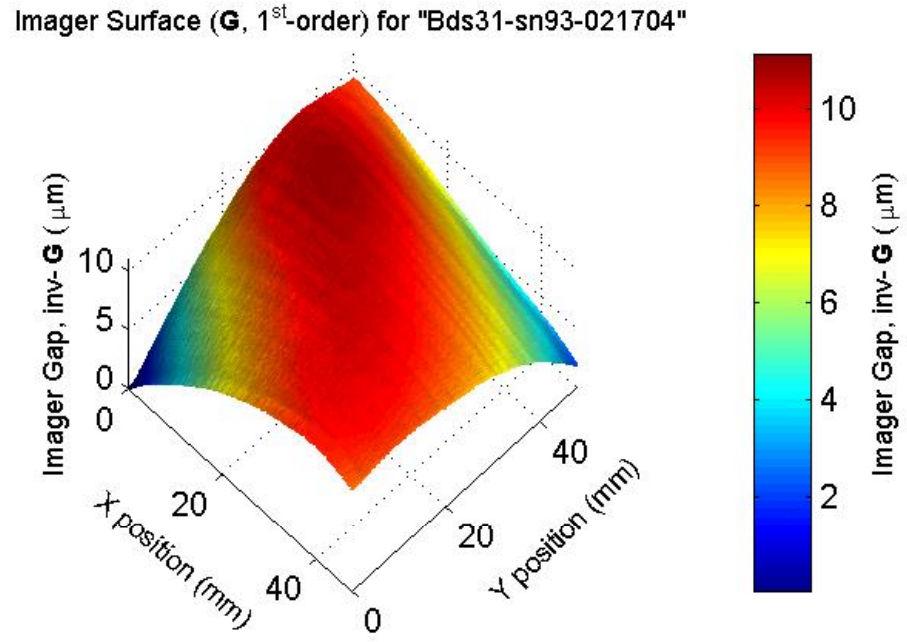
Some examples of profiles of some typical image sensors surfaces are shown below.



5x5 median filter, surface inverted, 1st-order leveled, offset (min/max was 1105.1/1112.2), Max=7.10, Left, Up



5x5 median filter, surface inverted, 1st-order leveled, offset (min/max was 1120.0/1128.8), Max=8.81, Left, Up



5x5 median filter, surface inverted, 1st-order leveled, offset (min/max was 1061.8/1072.9), Max=11.13, Left, Up

QUALITY ASSURANCE AND RELIABILITY

Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

Liability of the Customer: Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Cleanliness: Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed. The cover glass is highly susceptible to particles and other contamination. Touching the cover glass must be avoided. See ISS Application Note DS 00-009, Cover Glass Cleaning, for further information.

ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224 for handling recommendations.

Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

ORDERING INFORMATION

Available Part Configurations

Type	Description	Glass Configuration
KAF-4320E	Monochrome	Temporary clear glass cover.

Please contact Image Sensor Solutions for available part numbers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
A	Initial very preliminary release fro purposes of discussion.
B	Filled in timing conditions table, updated pin out and package drawings. These are new.
C	New package drawing. One dimension changed. Added some performance parameters that will need to be characterized. Added number designators to the outputs: Vout1, Vout2,…
D	Fixed incorrect pin descriptions in table 1. 28,29 and 35,36. Modified the clock signal level terminology to be consistant, specify a low level with a clock amplitude for all clock signals.
E	Updates with characterization results. Changed name to KAF-4320.
F	Changed H2 low level from –4 to –3 volts, updated dynamic range specs, removed noise floor at 1MHz pixel rate, fixed type in V1 clock levels,
G	Added CCD flatness specification. Removed description of KAF-4314 package.
1.0	First formal release.

PHYSICAL DESCRIPTION

Package Drawing

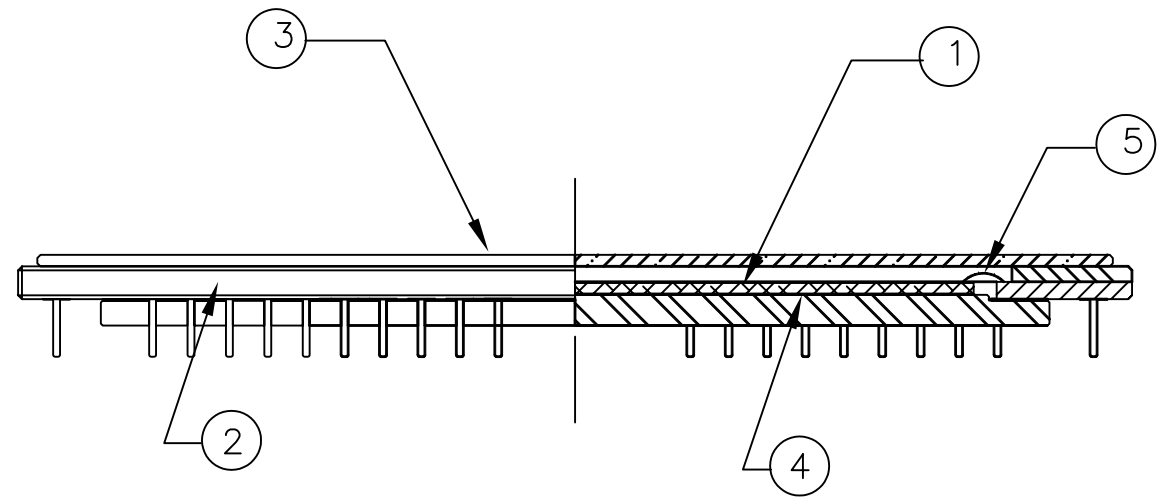
REVISION		
NO.	CHANGE	ECO/PCR # DATE

Table 1: KAF–4320xx Assembly Description and Parts List

PART NUMBER	MARKING CODE	DEVICE DESCRIPTION	DIE	PACKAGE ASSEMBLY	GLASS	D/A ADHESIVE	BOND WIRE
3F5038	KAF–4320E S31NE S/N	MONOCHROME, ITO, BUILT–UP PACKAGE, TAPED CLEAR GLASS	3F5039	3F5040	3E8366	7B5663	7B5463
		COMPONENT NUMBER	(1)	(2)	(3)	(4)	(5)

PIN FUNCTION TABLE

Pin	Func.	Pin	Func.	Pin	Func.	Pin	Func.
1	SUB	22	Vss	43	RD	64	Vlg
2	ΦR	23	Vlg	44	Sub	65	Sub
3	OG	24	Sub	45	ΦR	66	Vout
4	H1L	25	Vout	46	OG	67	Vdd
5	H1	26	Vdd	47	H1L	68	TF2
6	H2	27	TF2	48	H1	69	TF1
7	Sub	28	TF1	49	H2	70	Sub
8	Sub	29	Sub	50	Sub	71	V1
9	Sub	30	V1	51	Sub	72	V2
10	N/C	31	V2	52	Sub	73	GUARD
11	N/C	32	GUARD	53	Sub	74	V2
12	Sub	33	V2	54	Sub	75	V1
13	Sub	34	V1	55	Sub	76	Sub
14	Sub	35	Sub	56	H2	77	TF1
15	H2	36	TF1	57	H1	78	TF2
16	H1	37	TF2	58	H1L	79	Vdd
17	H1L	38	Vdd	59	OG	80	Vout
18	OG	39	Vout	60	ΦR	81	Sub
19	ΦR	40	Sub	61	Sub	82	Vlg
20	Sub	41	Vlg	62	RD	83	Vss
21	RD	42	Vss	63	Vss	84	RD



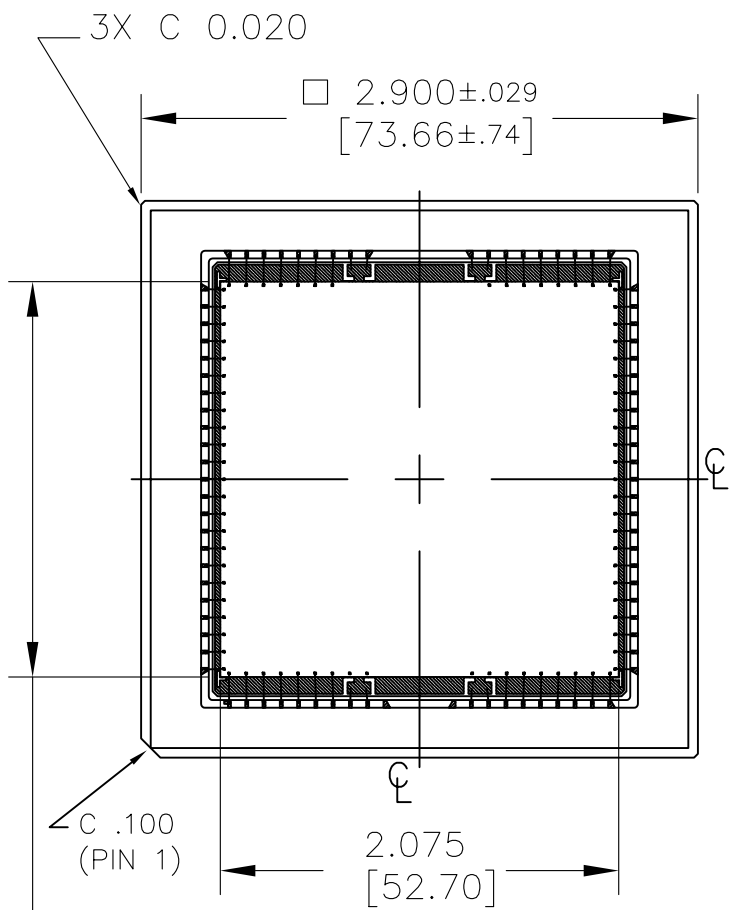
DIMENSIONS	UNITS: IN [MM]
TOLERANCE: UNLESS OTHERWISE SPECIFIED CERAMIC ±1% NO LESS THAN 0.005" L/F ±1% NO MORE THAN 0.005"	
APPROVALS	
DESIGNED BY: J. WALDMAN	DATE: 02/05/2004
DATE APPROVED: See KAF–4320xx in System–9000	

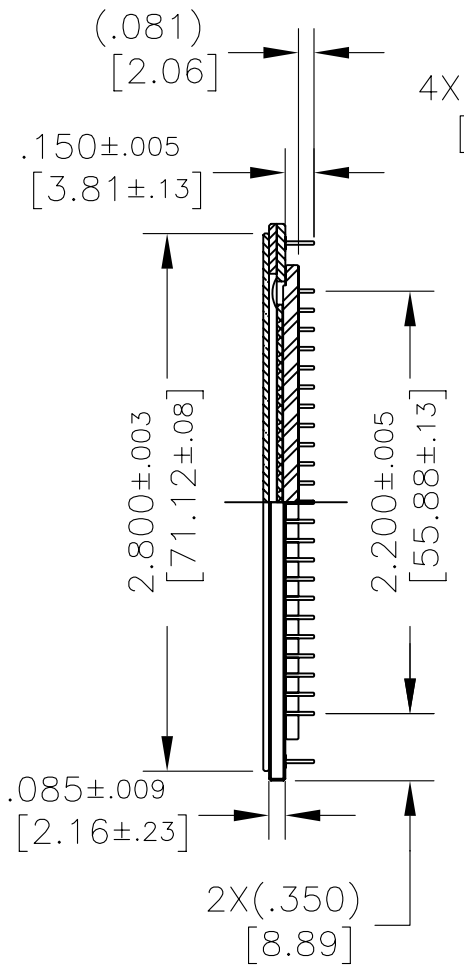
EASTMAN KODAK CO.
IMAGE SENSORS SOLUTIONS
ROCHESTER, NEW YORK

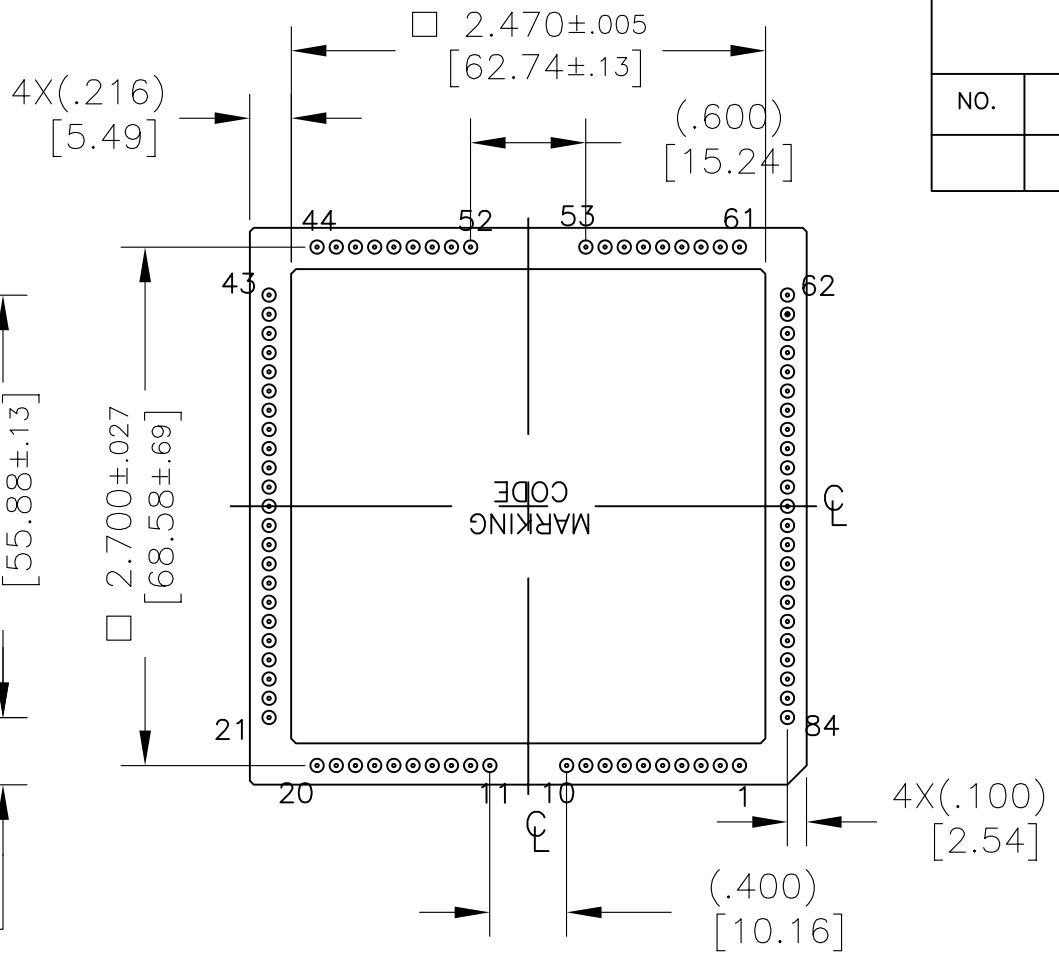
NAME
KAF–4320 / S31
ASSEMBLY

DRAWING NUMBER	REV.
KAF–4320xx	1

SHEET	DWG. SIZE
1 OF 3	B

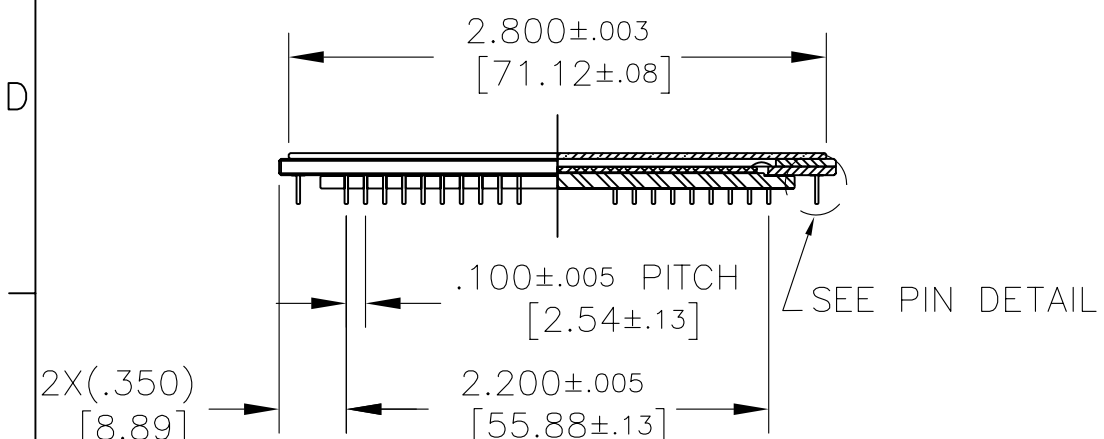


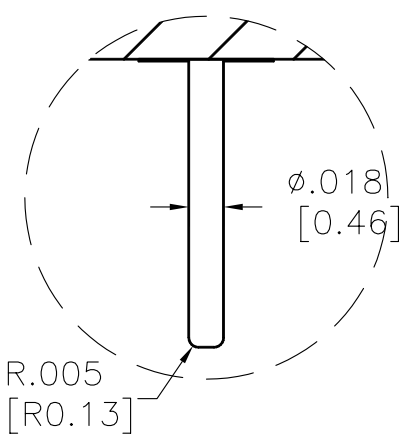




REVISION		
NO.	CHANGE	ECO/PCR # DATE

NOTES:
1. SEE TABLE 1 FOR MARKING CODE.
2. COVER GLASS IS VISUALLY ALIGNED OVER DIE – NO GUARANTEE OF LOCATION ACCURACY.





TYPICAL PIN DETAIL

DIMENSIONS	UNITS: IN [MM]
TOLERANCE: UNLESS OTHERWISE SPECIFIED CERAMIC ±1% NO LESS THAN 0.005" L/F ±1% NO MORE THAN 0.005"	
APPROVALS	
DESIGNED BY: J. WALDMAN	DATE: 02/05/2004
DATE APPROVED: See KAF-4320xx in System-9000	

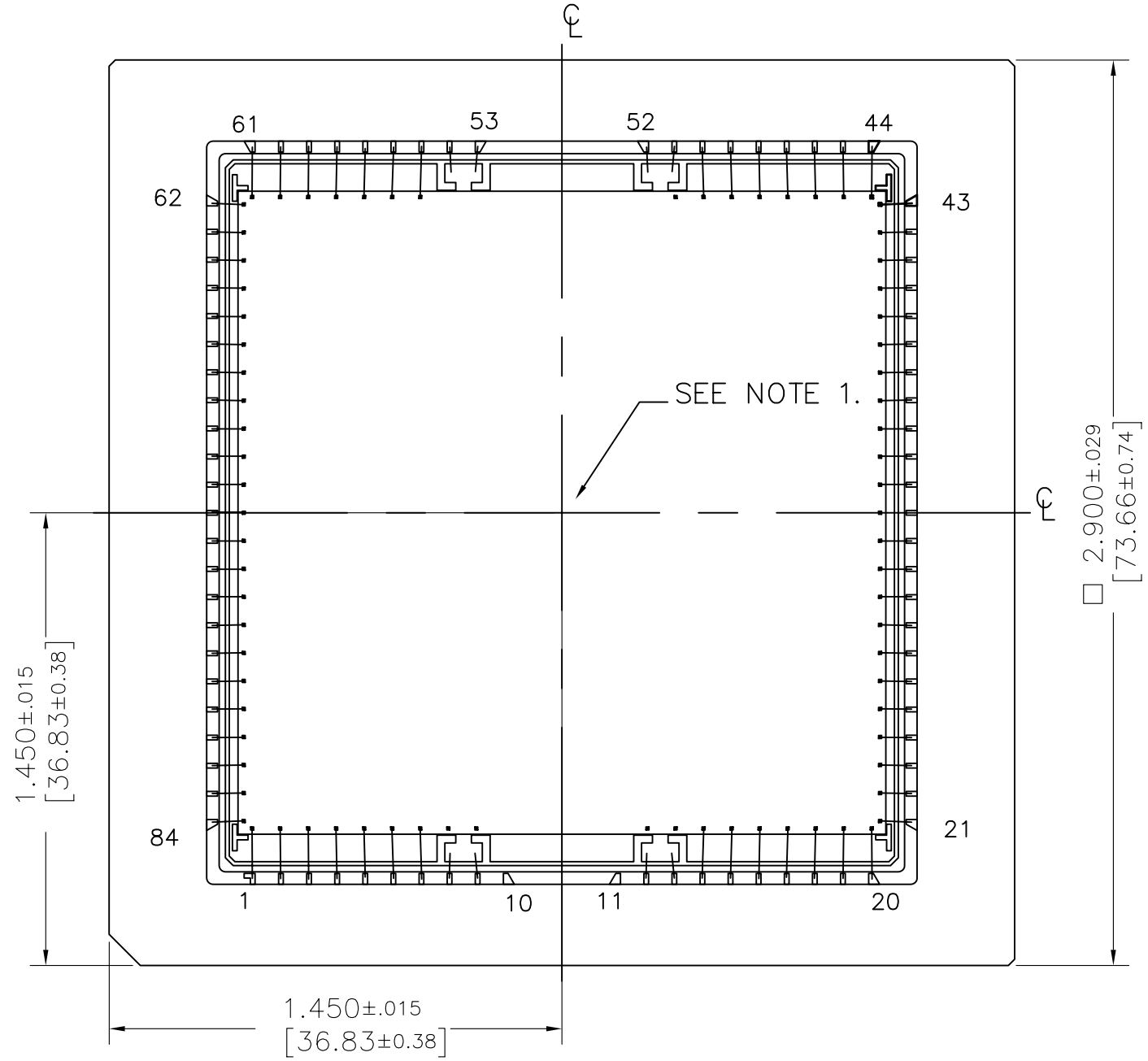
EASTMAN KODAK CO.
IMAGE SENSORS SOLUTIONS
ROCHESTER, NEW YORK

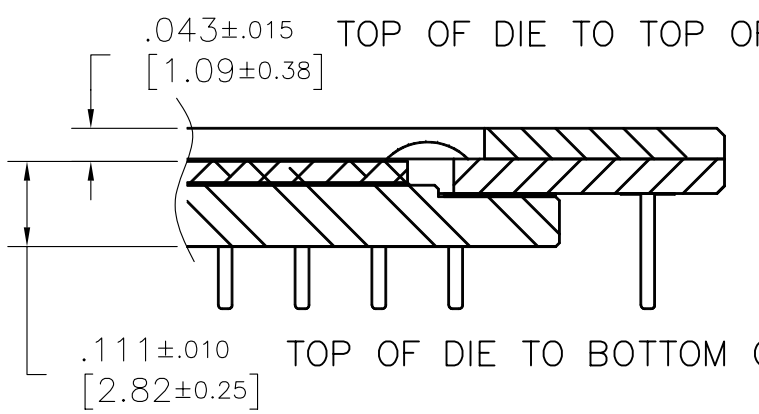
NAME
KAF-4320 / S31
ASSEMBLY

DRAWING NUMBER	REV.
KAF-4320xx	1

SHEET	DWG. SIZE
2 OF 3	B

REVISION		
NO.	CHANGE	ECO/PCR # DATE





NOTES:
1. CENTER OF IMAGE AREA IS OFFSET FROM CENTER OF PACKAGE BY (0.00,−0.00)mm NOMINAL.
2. DIE IS VISUALLY ALIGNED WITHIN ± 2° OF ANY PACKAGE CAVITY EDGE.

DIMENSIONS	UNITS: IN [MM]
TOLERANCE: UNLESS OTHERWISE SPECIFIED CERAMIC ±1% NO LESS THAN 0.005" L/F ±1% NO MORE THAN 0.005"	
APPROVALS	
DESIGNED BY: J.WALDMAN	DATE: 02/05/2004
DATE APPROVED: See KAF−4320xx in System−9000	

EASTMAN KODAK CO.
IMAGE SENSORS SOLUTIONS
ROCHESTER, NEW YORK

NAME
KAF−4320 / S31
ASSEMBLY

DRAWING NUMBER	REV.
KAF−4320xx	1

SHEET	DWG. SIZE
3 OF 3	B